IN THE CLAIMS

1. (Currently amended) A data processing device configured according to a device configuration so as to be capable of executing a program comprising an instruction, the device comprising a configurable functional unit for executing the instruction according to a configurable function that is configured outside the instruction, the configurable functional unit having

- a unit input and a unit output for inputting and outputting bits of an operand and a result to a source and destination register specified by the instruction respectively, the configurable function unit comprising

- a plurality of independent configurable logic blocks for performing programmable logic operations to implement the configurable function and producing outputs having a relative order;

- a first programmable connection circuit between the unit input and the logic blocks, for selectively coupling inputs of the logic blocks to bits from the unit input, dependent on the configured function;

- a second programmable connection circuit between the logic blocks and the unit output, for selectively coupling bits of the unit output to outputs of the logic blocks, dependent on the configured function;

wherein, for at least one configured function, the second programmable connection circuit reverses the relative order of outputs of different logic blocks.

~~wherein more than one instruction is implemented with the same configuration.~~

2. (Previously presented) A data processing device according to Claim 1, each logic block having a plurality of outputs, at least one of the bits of the unit output being connectable exclusively to one of the outputs of each logic block, the second programmable connection circuit comprising a multiplexer for coupling the one of the outputs of a selected one of the logic blocks to the at least one of the bits of the unit output.

3. (Previously presented) A data processing device according to Claim 2, each logic bock having a plurality of outputs, each of the bits of the unit being connectable exclusively to a respective one of the outputs of each logic block, the second programmable connection circuit comprising a respective multiplexer for each particular bit of the unit output, for coupling the respective one of the outputs of a selected one of the logic blocks to the particular bit of the unit output.

4. (Previously presented) A data processing device according to Claim 1, either the first programmable connection circuit or the second programmable connection circuit having a fixed, unprogrammable connection to an input or output of one of the independent configurable logic blocks and a programmable connection to a remainder of the inputs and outputs.

5. (Currently amended) A method of programming a configurable processing device according to a device configuration to perform a processing task, wherein the device has a configurable processing unit that comprises several programmable logic blocks, the method comprising
- identifying a special complex of operations that occurs in the task and requires an operand data word and produces a result data word;
- searching for an assignment of the logic operations for producing different bits of the result to different ones of the programmable logic blocks, so that the logic operations for producing a subset of the bits of the result that, if implemented together in one of the programmable logic blocks, would exceed the capacity of that one of the programmable logic blocks, are distributed over different ones of the logic blocks;
- programming each of the programmable logic blocks to perform the logic operations for the bits of the result assigned to it;
-programming connection circuits in from of the programmable logic blocks and subsequent to the logic blocks so as to ~~route~~ perform a first routing of bits of an operand of a special instruction to the programmable logic blocks that use those bits of the operand in the logic operations and so as to ~~route~~ perform a second routing

outputs of the programmable logic blocks to bits of the result to which the programmable logic blocks are assigned;

wherein, for at least one configured function, a relative order of outputs of different logic blocks is reversed during said second routing.

~~wherein the special complex of operations includes multiple instructions implemented with the same configuration~~.

6. (Currently amended) A method of executing a program with a processing device with a configurable functional unit according to a device configuration, the method comprising executing the following steps in response to a configurable instruction

- inputting bits of an operand of the configurable instruction into the configurable functional unit;
- selectively coupling the bits of the operands to inputs of logic blocks, dependent on a configured function;
- performing programmable logic operations to implement the configurable function;
- selectively coupling outputs of the logic blocks to bits of a result, dependent on a configured function;

wherein, for at least one configured function, a relative order of outputs of different logic blocks is reversed during said selectively coupling outputs.

~~wherein more than one instruction is implemented with the same configuration~~.